



FIG. 1A

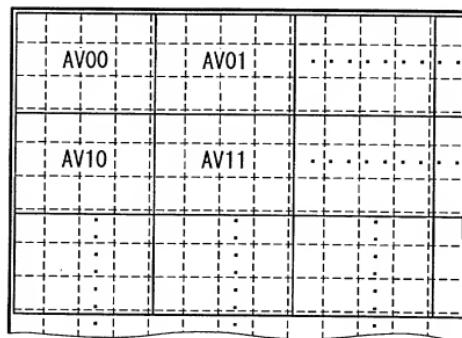


FIG. 1B

平均化開始位置

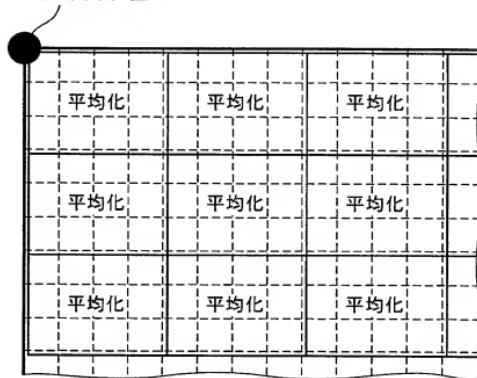


FIG. 2A

平均化開始位置

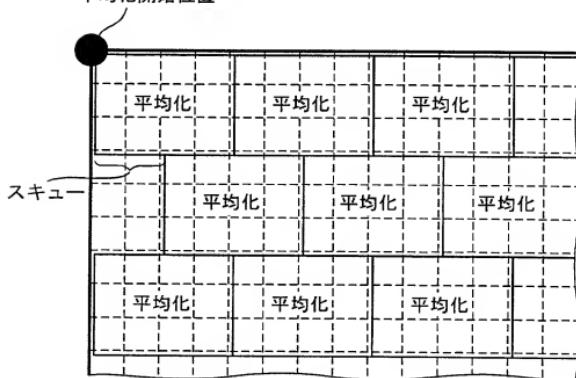


FIG. 2B

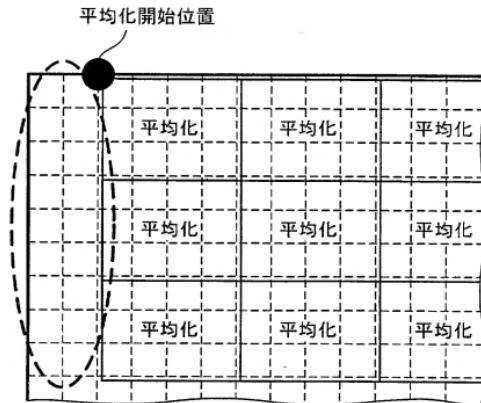


FIG. 3A

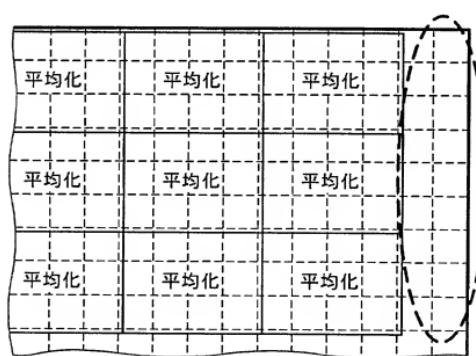


FIG. 3B

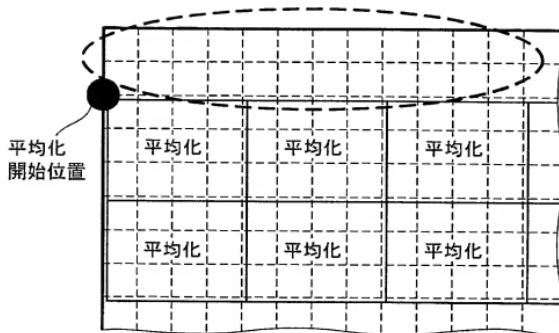


FIG. 3C

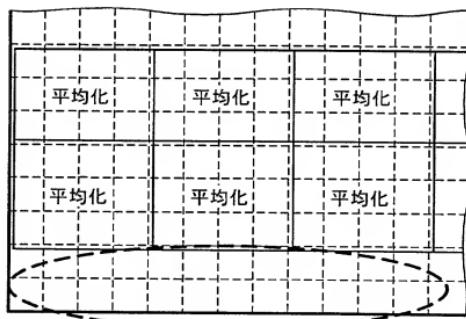


FIG. 3D

1085-1086 • J. Neurosci., March 22, 2006 • 26(12):1083–1086

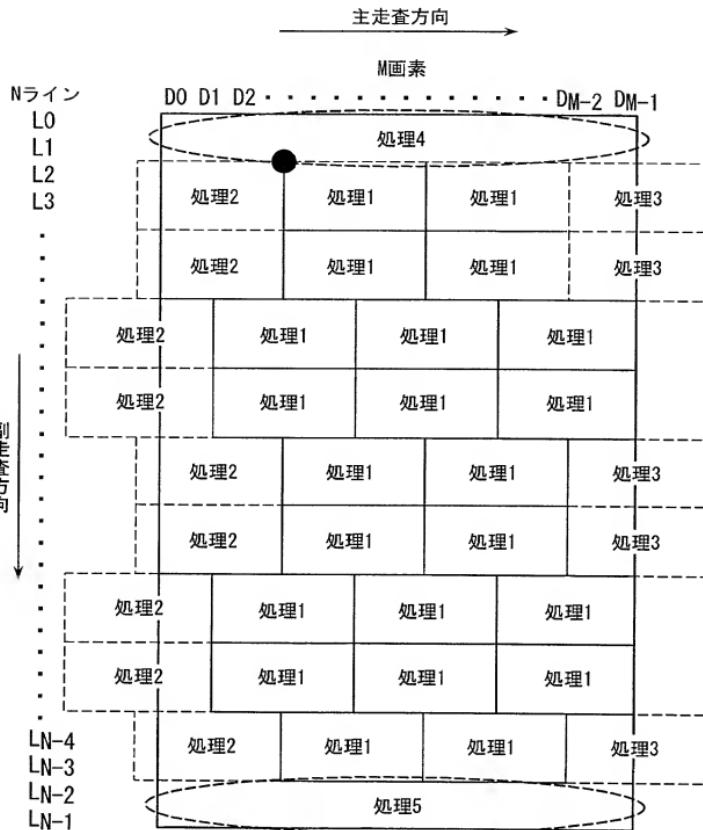


FIG. 4

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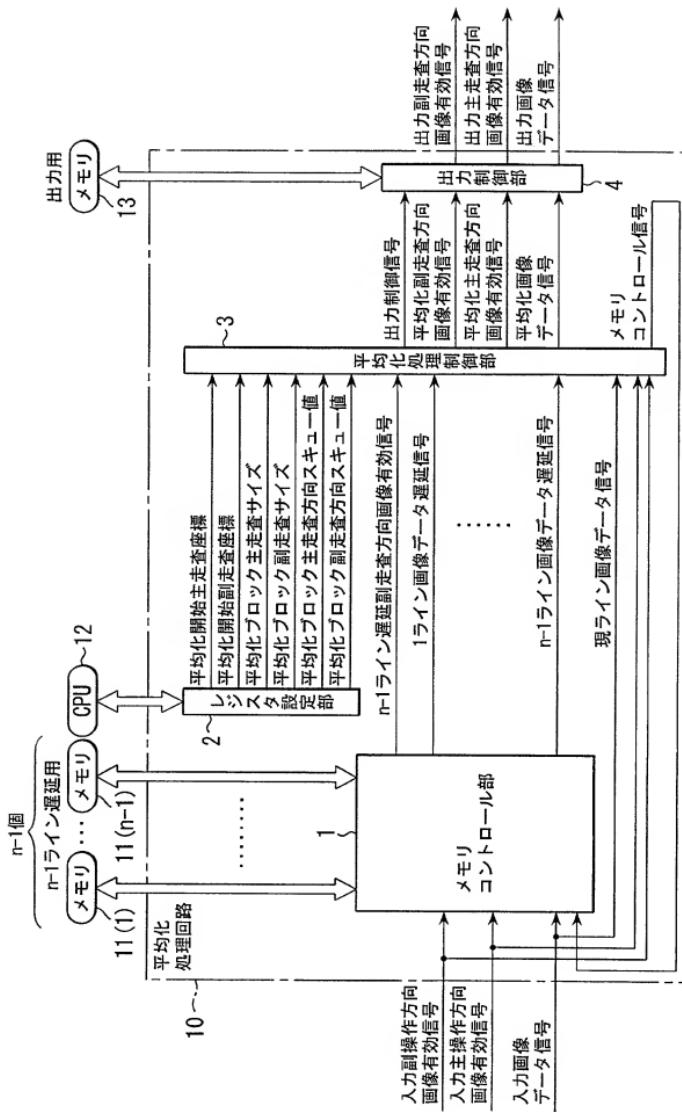


FIG. 5

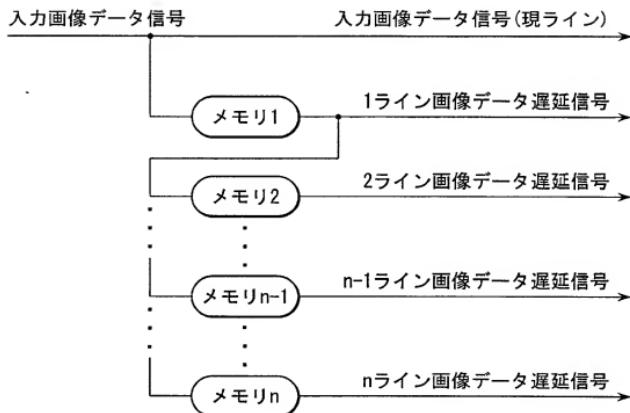


FIG. 6A

卷之三

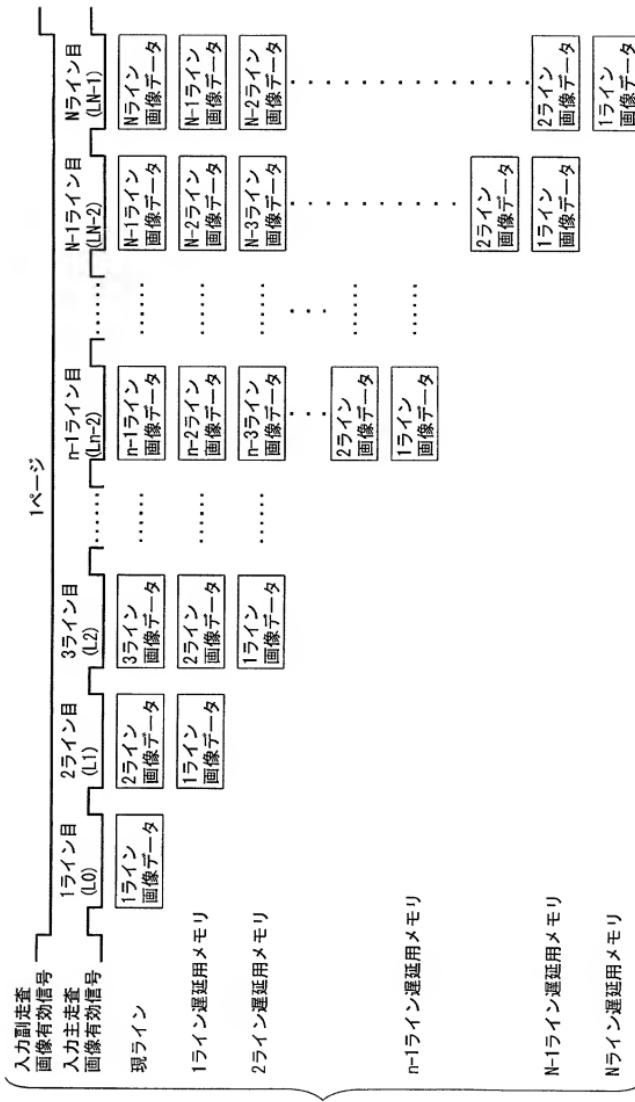


FIG 6B

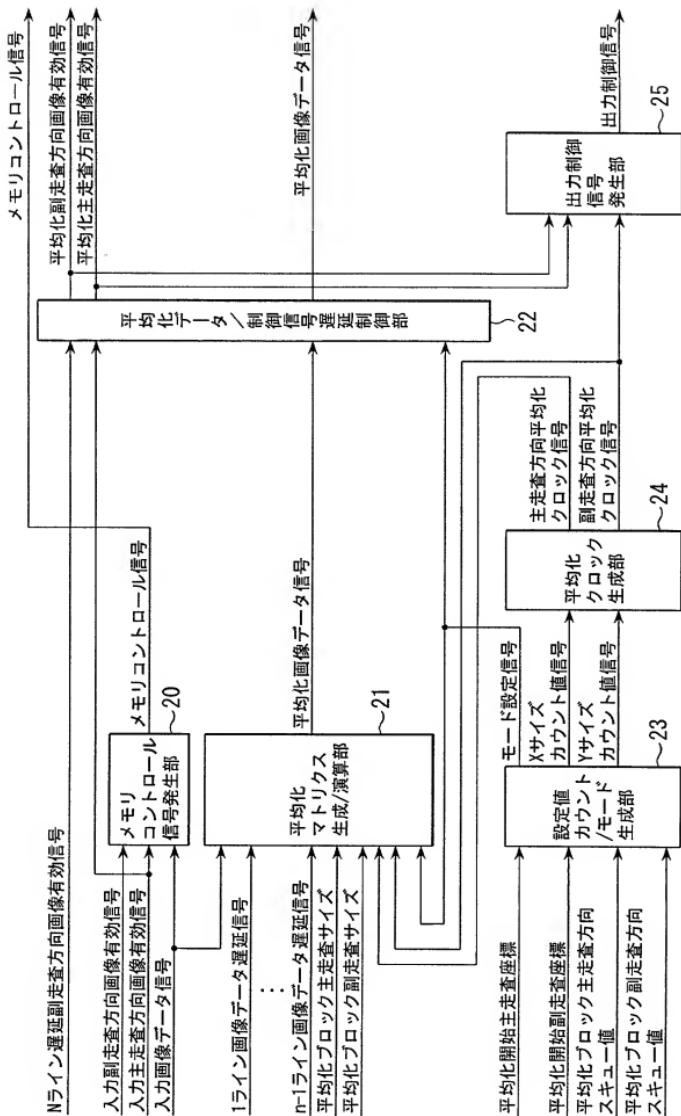


FIG. 7

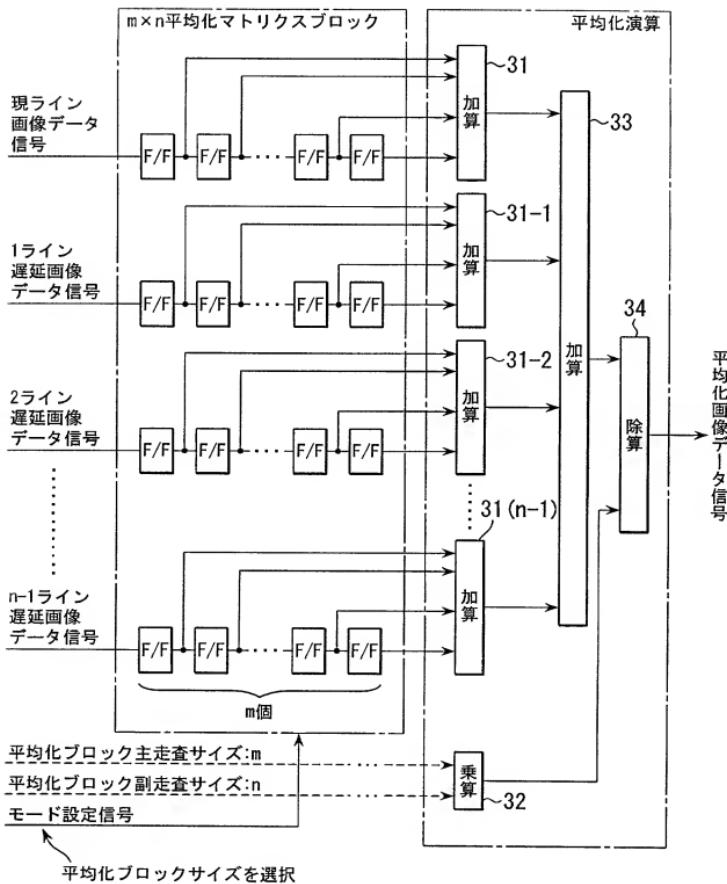
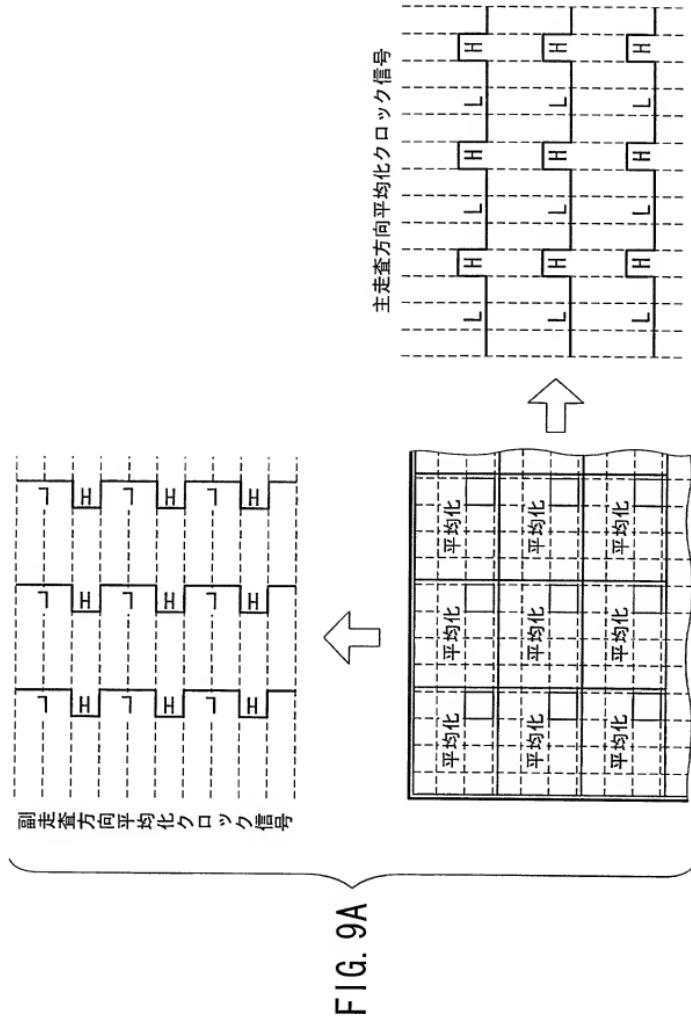


FIG. 8

1055-0212



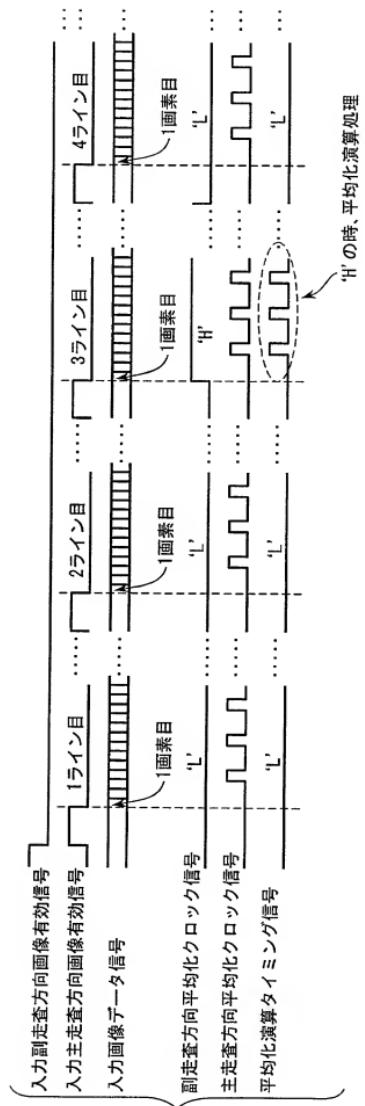


FIG. 9B

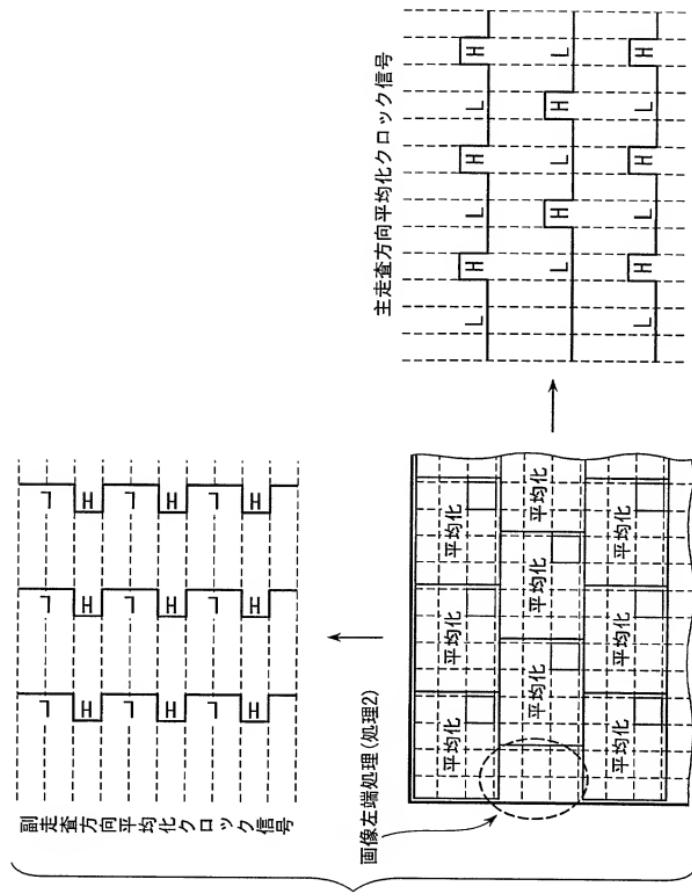
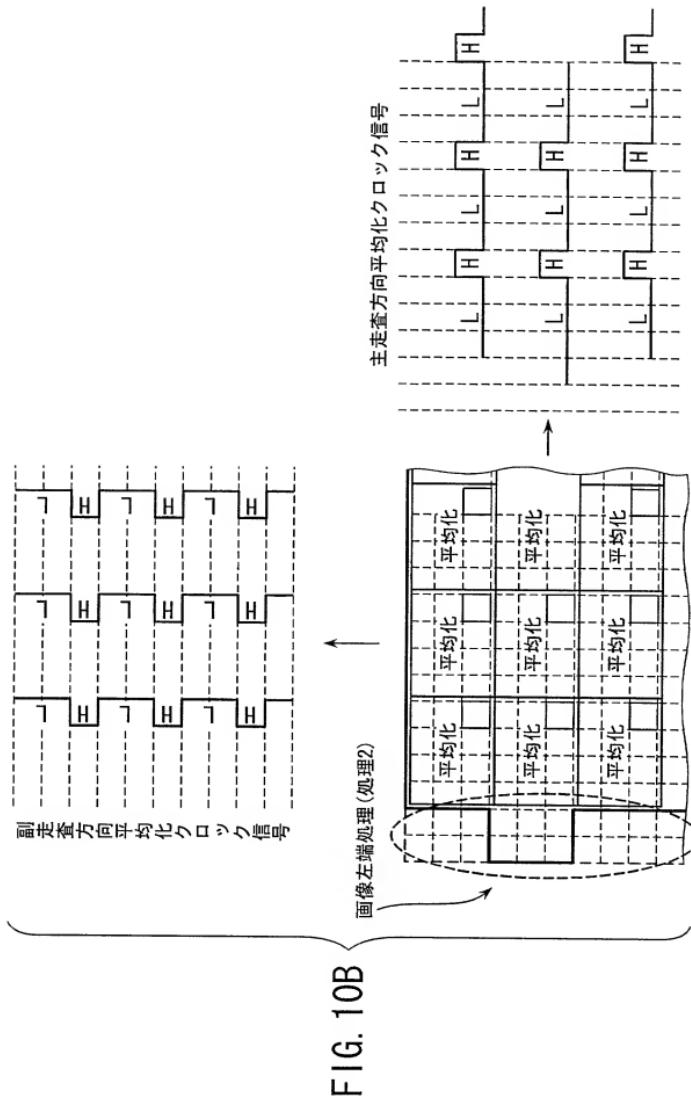


FIG. 10A

2052010-20455007



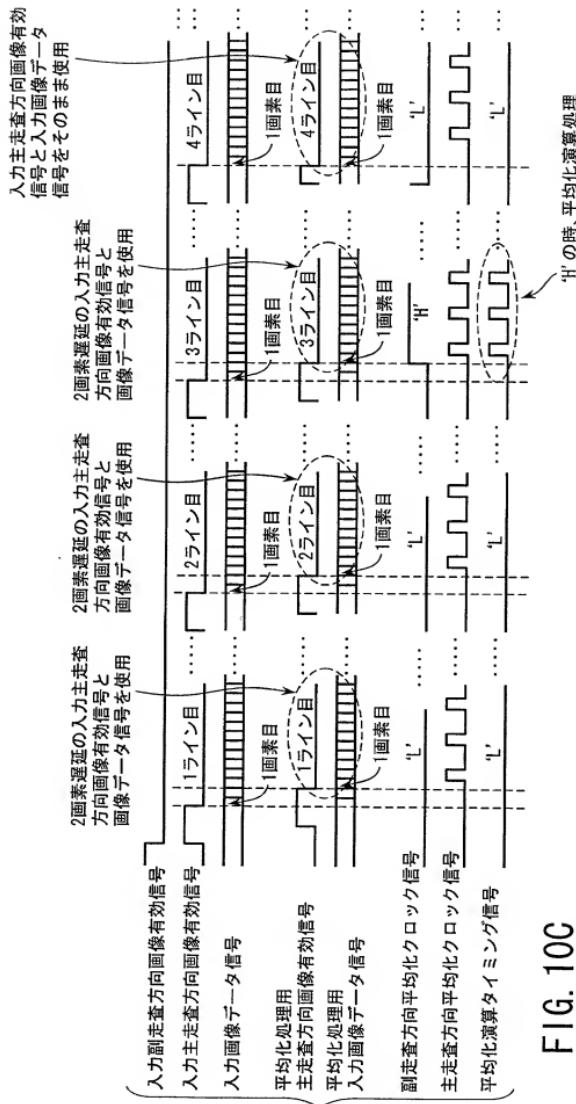


FIG. 10C

三〇〇五四〇二・三〇〇五四〇二

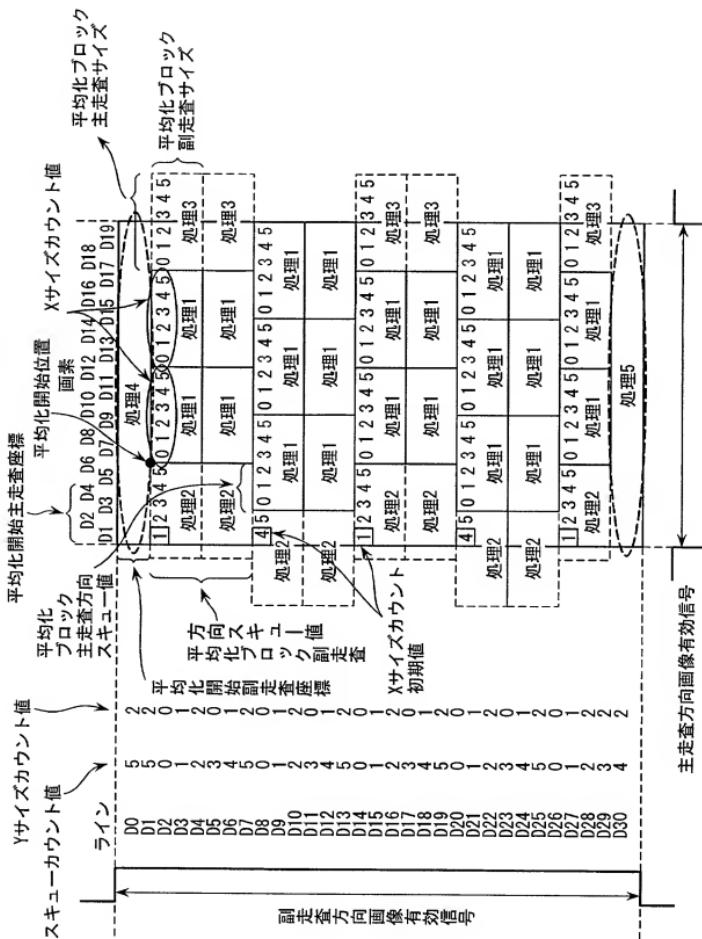


FIG. 1

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Figure 10-10 is a timing diagram illustrating the processing timing of a 5-stage image processing system. The diagram is divided into three main sections: '副走査方向平均化' (Side Scan Direction Averaging), '主走査方向平均化' (Main Scan Direction Averaging), and '平均化主走査方向画像有効信号' (Averaged Main Scan Direction Image Valid Signal).

**副走査方向平均化 (Side Scan Direction Averaging):** This section shows the 'Yサイズカウント値' (Y size count value) on the left, which is a digital signal with a period of 2. The diagram is divided into 5 horizontal rows, each representing a frame. Each frame is further divided into 5 vertical columns, labeled 0 to 4. The processing steps are as follows:

- Row 1:** '処理2' (Processing 2) is active for columns 0 to 4. '処理1' (Processing 1) is active for column 5.
- Row 2:** '処理2' (Processing 2) is active for columns 0 to 4. '処理1' (Processing 1) is active for column 5.
- Row 3:** '処理2' (Processing 2) is active for columns 0 to 4. '処理1' (Processing 1) is active for column 5.
- Row 4:** '処理2' (Processing 2) is active for columns 0 to 4. '処理1' (Processing 1) is active for column 5.
- Row 5:** '処理2' (Processing 2) is active for columns 0 to 4. '処理1' (Processing 1) is active for column 5.

**主走査方向平均化 (Main Scan Direction Averaging):** This section shows the '主走査方向平均化クロック信号' (Main Scan Direction Averaging Clock Signal) and '入力主走査方向画像有効信号' (Input Main Scan Direction Image Valid Signal). The clock signal has a period of 2. The diagram shows the processing steps for each frame:

- Row 1:** '処理5' (Processing 5) is active for columns 0 to 4. '処理3' (Processing 3) is active for column 5.
- Row 2:** '処理5' (Processing 5) is active for columns 0 to 4. '処理3' (Processing 3) is active for column 5.
- Row 3:** '処理5' (Processing 5) is active for columns 0 to 4. '処理3' (Processing 3) is active for column 5.
- Row 4:** '処理5' (Processing 5) is active for columns 0 to 4. '処理3' (Processing 3) is active for column 5.
- Row 5:** '処理5' (Processing 5) is active for columns 0 to 4. '処理3' (Processing 3) is active for column 5.

**平均化主走査方向画像有効信号 (Averaged Main Scan Direction Image Valid Signal):** This section shows the 'モード設定信号' (Mode Setting Signal) and the resulting '平均化主走査方向画像有効信号' (Averaged Main Scan Direction Image Valid Signal). The mode setting signal has a period of 2. The averaged signal is shown as a solid line.

**注記 (Notes):**

- (処理2の例) 左端画像データ (D0) を使用して 平均化処理を行う
- (処理4の例) 上端画像データは スルー出力する
- (処理3の例) 右端画像データ (D19) を使用して 平均化処理を行う
- (処理5の例) 下端画像 データは スルー 出力する

FIG. 12

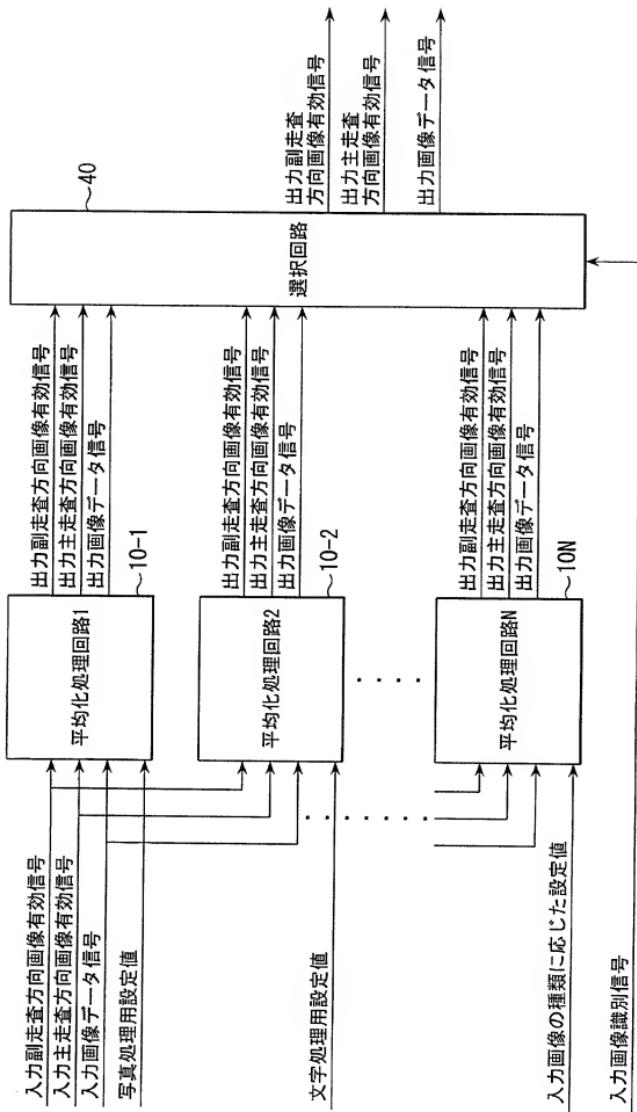


FIG. 13

この信号により画像が写真、文字など識別されている。

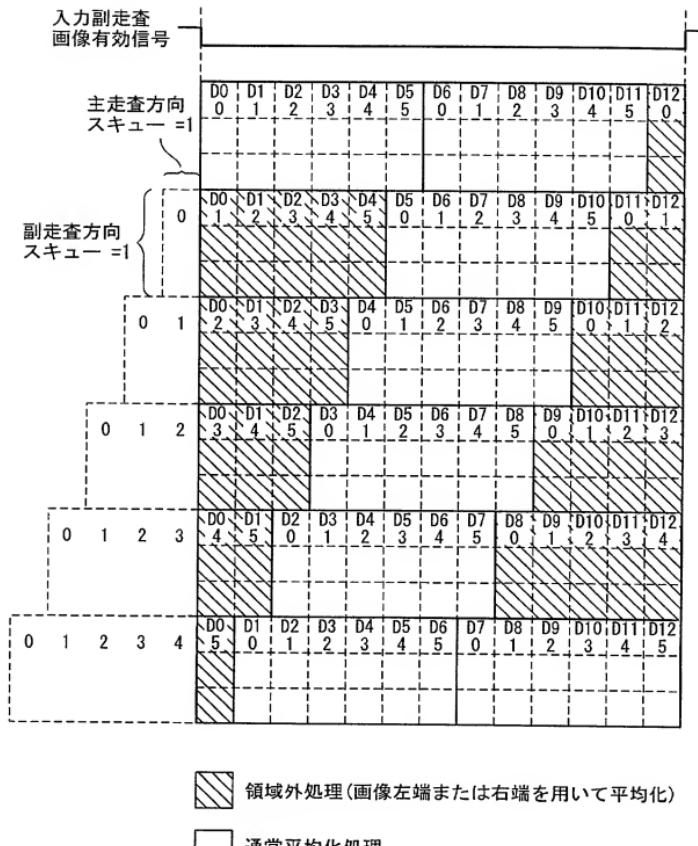


FIG. 14

10055402 · 012502

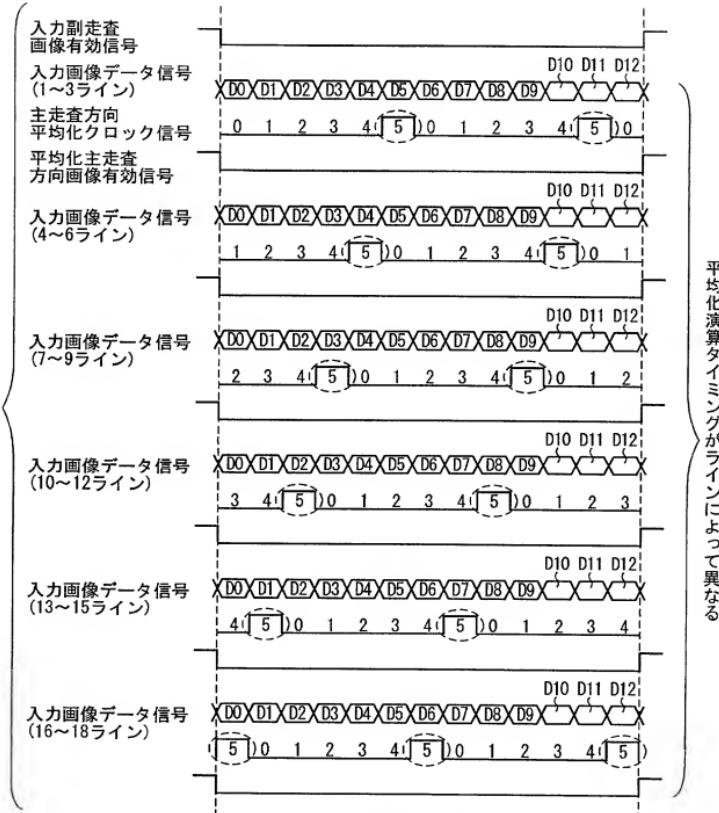


FIG. 15

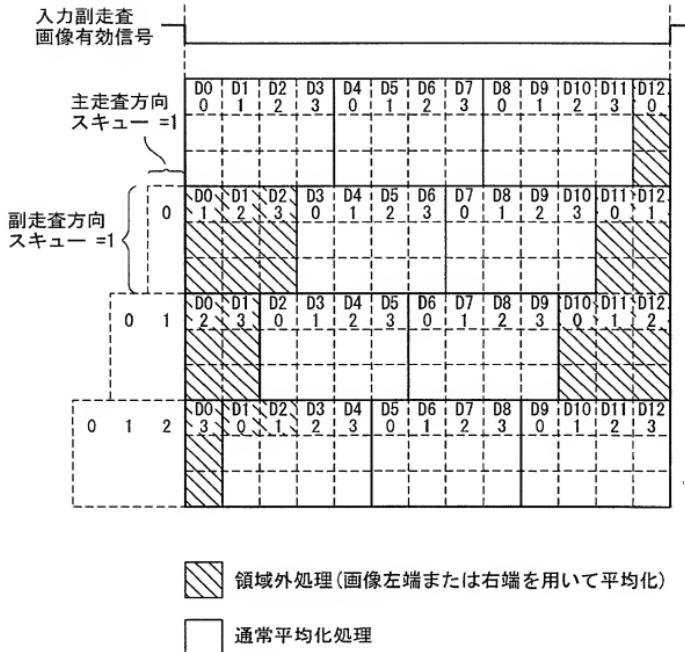


FIG. 16

205210-20455001

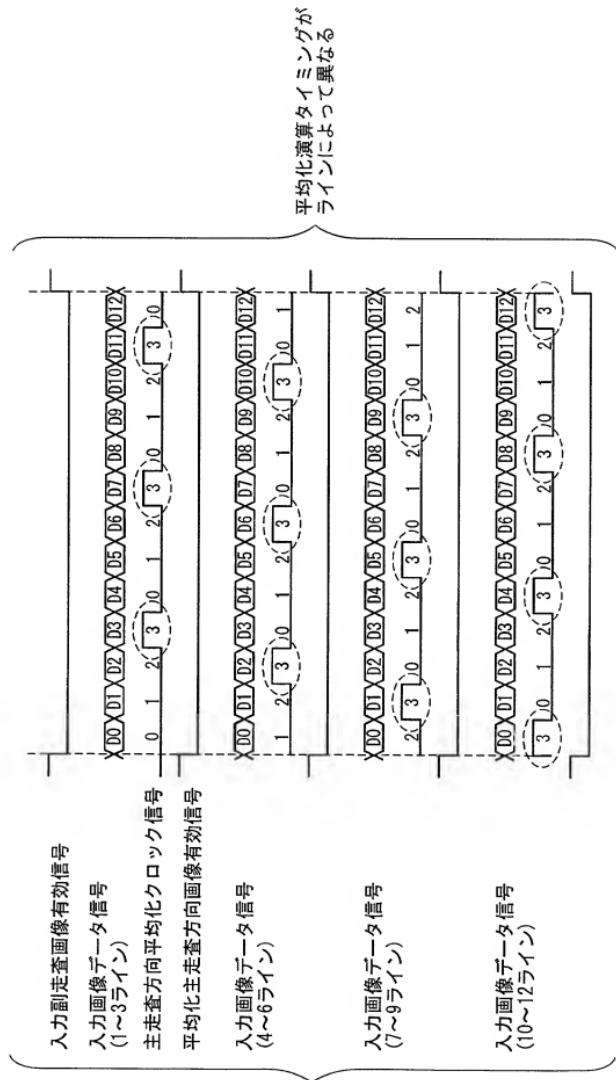


FIG. 17

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### 输入副走查画像有效信号

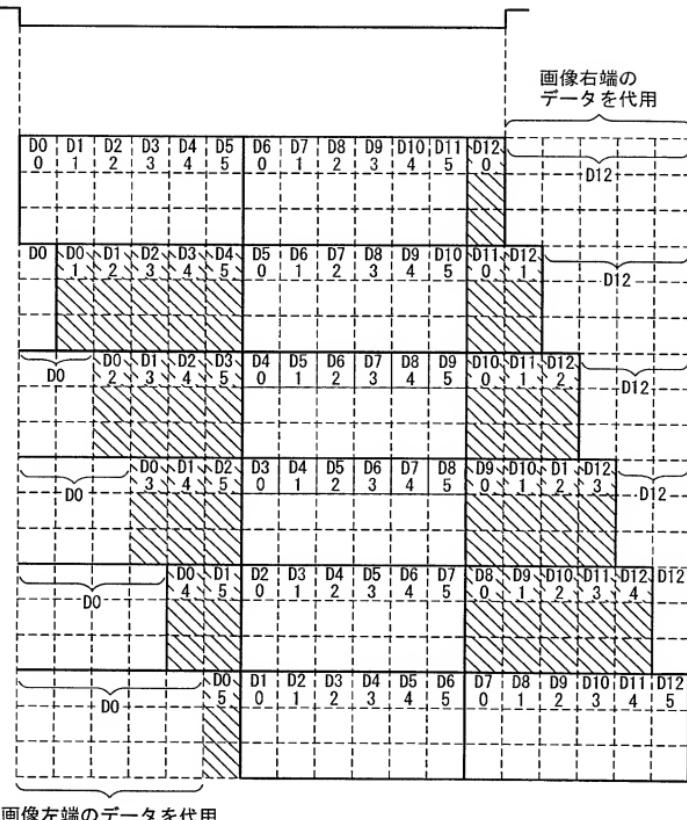


FIG. 18

1035402-012602905007

処理するラインにより遅延調整を行う。

205ATO "2045500T

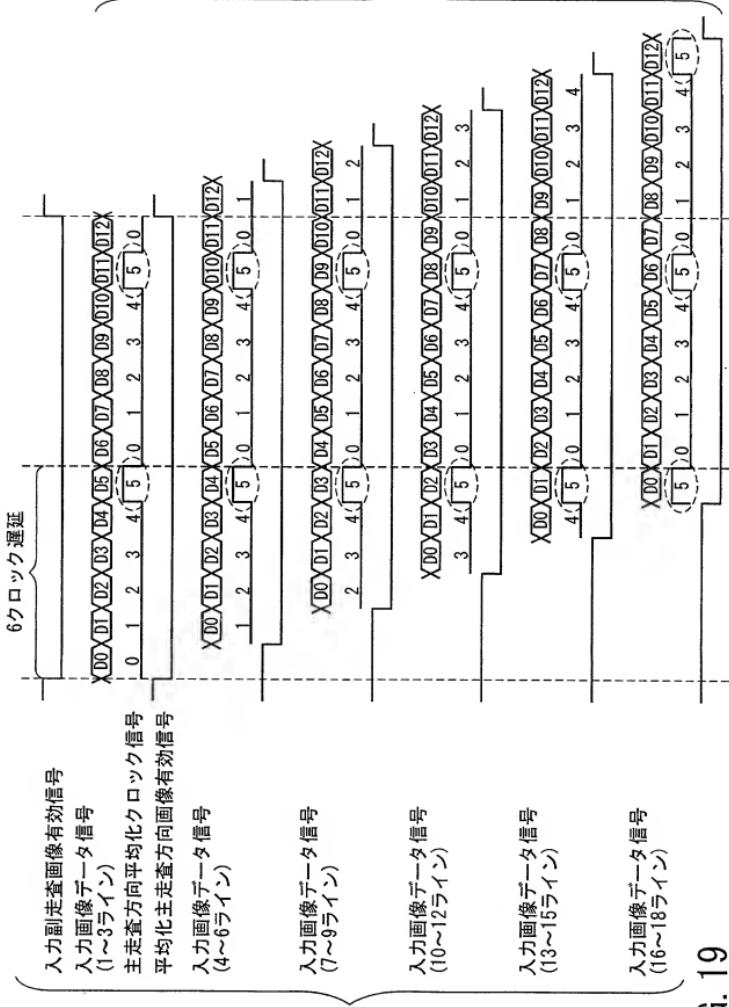


FIG. 19

入力副走査画像有効信号

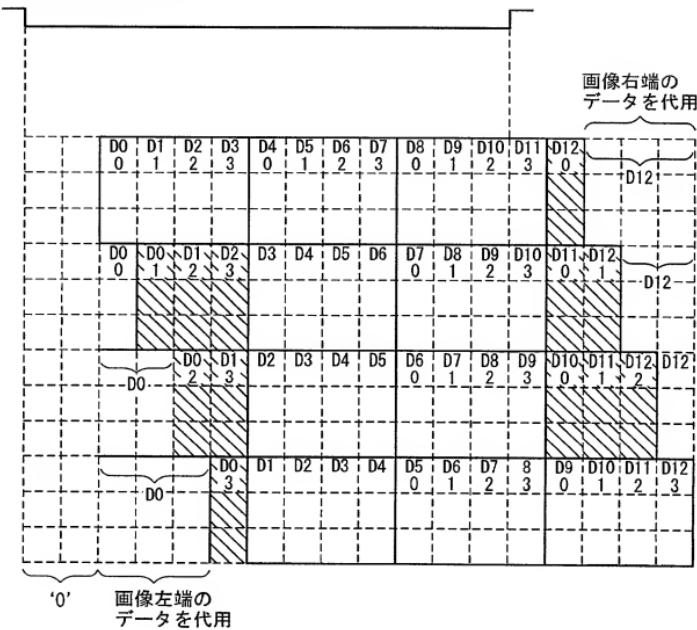


FIG. 20

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**CIRCUIT AND METHOD**  
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**DOCKET NO. 016907/1365**

処理するライン上に遅延調整を行う。

205200-2045500T

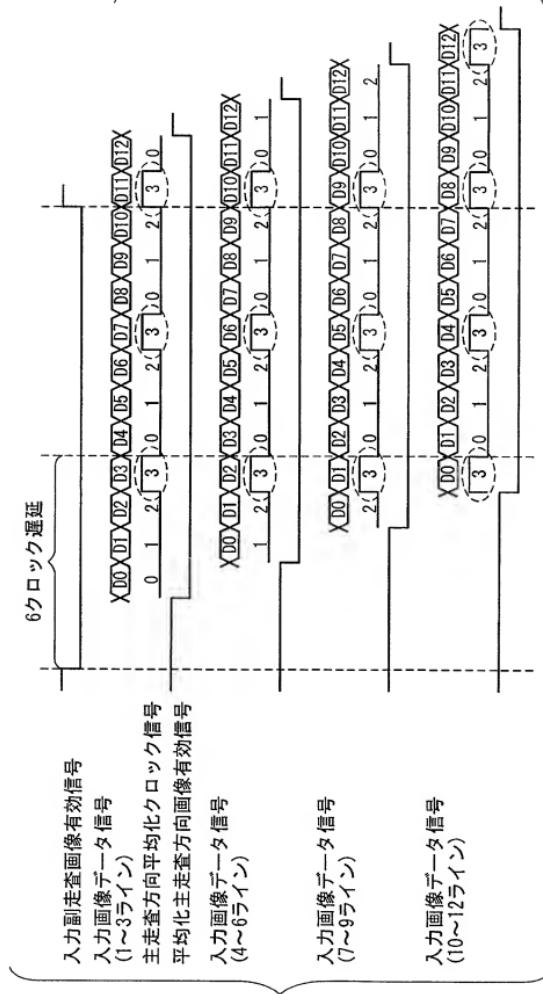
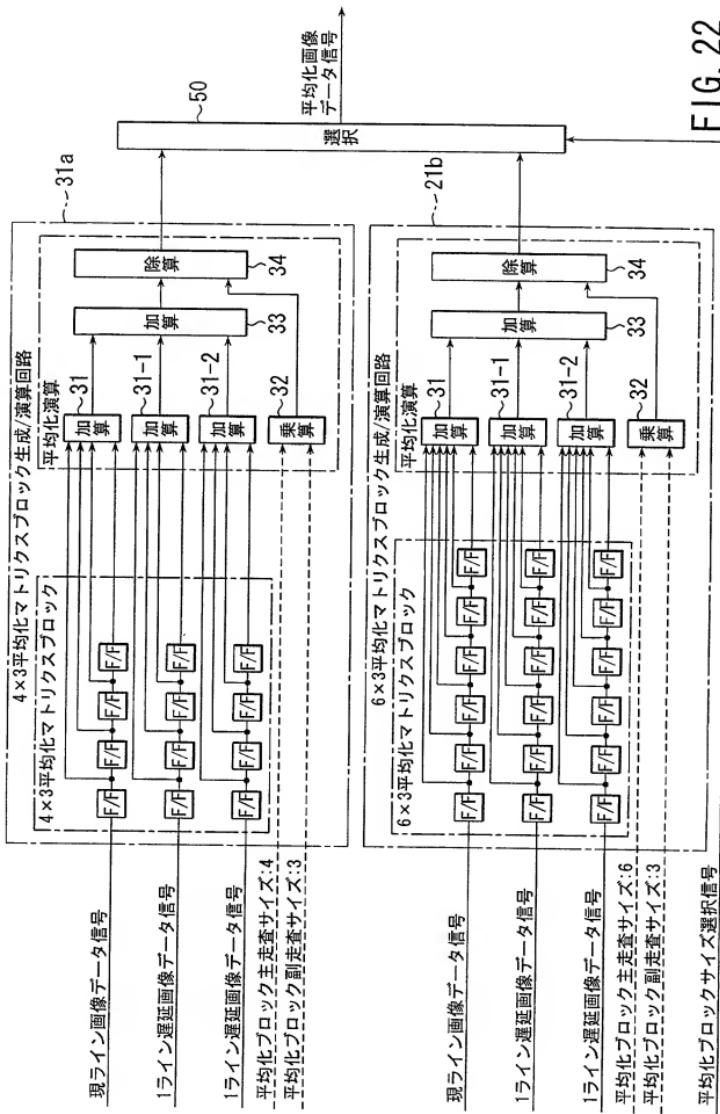


FIG. 21

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CIRCUIT AND METHOD  
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DOCKET NO. 016907/1365

1985-86



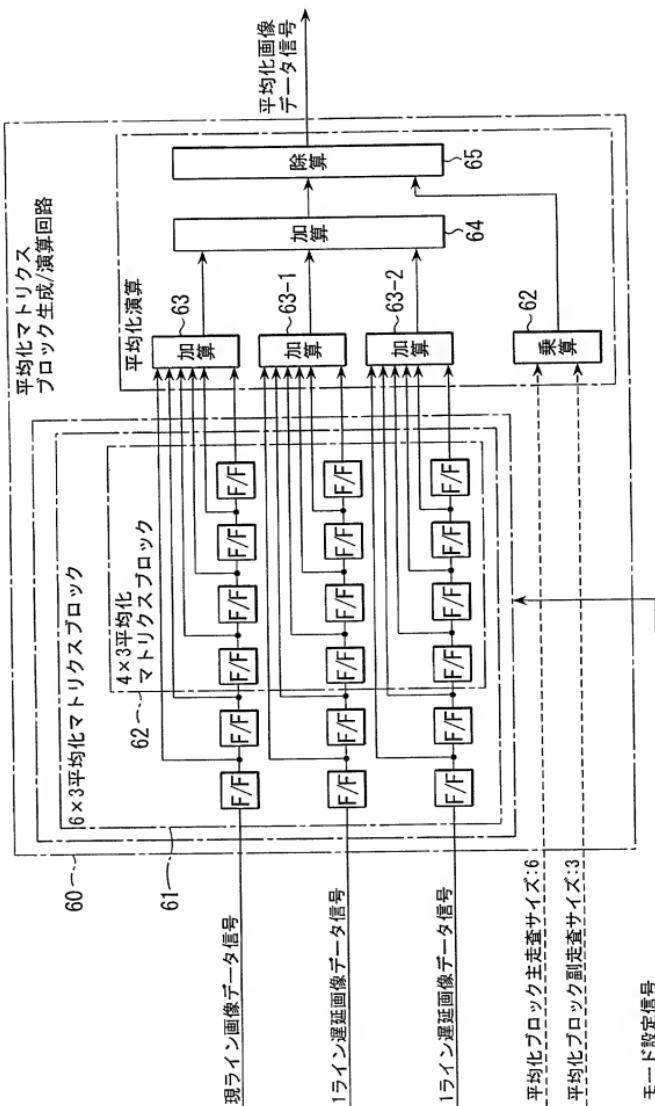


FIG. 23